[0330] With this configuration, variations of the width of the diode trench and the width of the gate trench can be kept within a specified range. Therefore, the occurrence of dishing in the gate electrode and the double-ended zener diode (the buried layer), e.g., when etching back the semiconductor material, can be prevented.

[0331] As recited in (16), the double-ended zener diode may be made of polysilicon.

[0332] By using polysilicon as an electrode material, the semiconductor device can be more easily and cost-effectively manufactured.

[0333] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosures. Indeed, the novel devices and methods described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the disclosures. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosures.

What is claimed is:

1. A semiconductor device, comprising:

a first-conductivity-type semiconductor layer including an active region in which a transistor having a plurality of impurity regions is formed and a marginal region surrounding an outer periphery of the active region;

a second-conductivity-type channel layer formed between the active region and the marginal region so as to form a front surface of the semiconductor layer;

at least one gate trench formed in the active region to extend from the front surface of the semiconductor layer through the channel layer;

a gate insulation film formed on an inner surface of the at least one gate trench;

a gate electrode formed inside the gate insulation film in the at least one gate trench; and

at least one isolation trench arranged between the active region and the marginal region to surround the outer periphery of the active region and formed to extend from the front surface of the semiconductor layer through the channel layer, the at least one isolation trench having a depth equal to a depth of the at least one gate trench.

2. The device of claim **1**, further comprising:

a trench insulation film formed on an inner surface of the at least one isolation trench; and

a buried electrode formed inside the trench insulation film in the at least one isolation trench.

3. The device of claim **1**, further comprising:

a first-conductivity-type high-concentration impurity region formed on a bottom surface of the at least one isolation trench,

wherein an impurity concentration of the high-concentration impurity region is higher than an impurity concentration of the semiconductor layer.

4. The device of claim **1**, further comprising:

an inter-layer insulation film formed on the semiconductor layer;

a first terminal formed on the inter-layer insulation film and connected to the gate electrode through the inter-layer insulation film; and

a second terminal formed on the inter-layer insulation film and connected to one of the impurity regions of the transistor through the inter-layer insulation film,

wherein the at least one isolation trench is positioned directly below the second terminal.

5. The device of claim **4**, further comprising:

a trench insulation film formed on an inner surface of the at least one isolation trench; and

a buried electrode formed inside the trench insulation film in the at least one isolation trench,

wherein the second terminal is connected through the inter-layer insulation film to the buried electrode of the at least one isolation trench arranged directly below the second terminal.

6. The device of claim **1**, wherein the at least one isolation trench includes a plurality of isolation trenches differing in perimeter from one another.

7. The device of claim **6**, wherein the second terminal is connected to the buried electrode disposed closest to the active region among the buried electrodes formed in the plurality of isolation trenches.

8. The device of claim **7**, wherein a width of the buried electrode connected to the second terminal is larger than a width of the remaining buried electrodes not connected to the second terminal.

9. The device of claim **6**, wherein the width of the isolation trenches is uniform.

10. The device of claim **6**, wherein a pitch of the isolation trenches decreases as the isolation trenches extend from the active region toward the marginal region.

11. The device of claim **6**, wherein a pitch of the isolation trenches increases as the isolation trenches extend from the active region toward the marginal region.

12. The device of claim **6**, wherein a pitch of the isolation trenches is uniform.

13. The device of claim **6**, wherein a pitch of the isolation trenches is smaller than a pitch of the gate trench.

14. The device of claim **6**, wherein a pitch of the isolation trenches is from 0.3 μm to 5.0 μm.

15. The device of claim **1**, wherein the number of the at least one isolation trench is one.

16. The device of claim **1**, further comprising:

an inter-layer insulation film formed on the semiconductor layer;

a first terminal formed on the inter-layer insulation film and connected to the gate electrode through the inter-layer insulation film; and

a second terminal formed on the inter-layer insulation film and connected to one of the impurity regions of the transistor through the inter-layer insulation film,

wherein the at least one isolation trench is positioned directly below the first terminal.

17. The device of claim **1**, further comprising:

a first-conductivity-type high-concentration impurity region formed on a bottom surface of the at least one gate trench,

wherein an impurity concentration of the high-concentration impurity region is greater than an impurity concentration of the semiconductor layer.

18. The device of claim **4**, wherein the second terminal is formed to cover the active region and the first terminal includes a gate pad to which a bonding wire is connected, the